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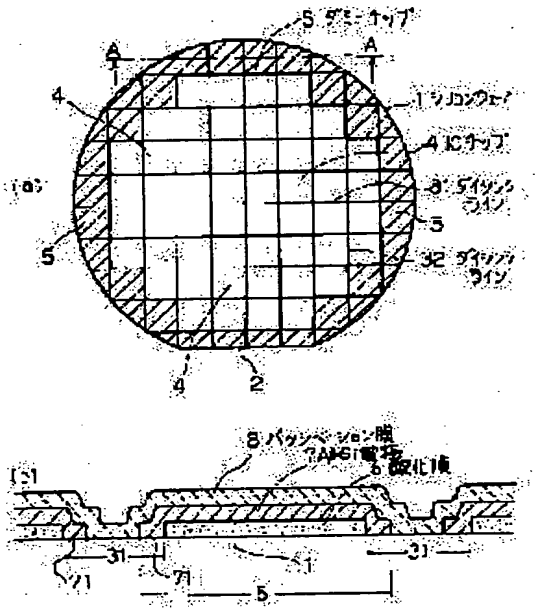
(54) MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To form a final passivation film of uniform quality on a semiconductor substrate by a method wherein a plasma CVD process is carried out bringing one of parallel electrodes into contact with the surface of an electrode layer formed on the peripheral surface of the semiconductor substrate where a film is formed.
CONSTITUTION: In dummy chips 5, an oxide film 6 formed on the surface of a wafer 1 is removed in lines for the formation of dicing lines 31 and 32 on the wafer 1, and an Al-Si electrode 7 is brought into contact with a part of the exposed region of the wafer 1 where the dicing line is provided. A plasma CVD method is carried out through such a manner that the wafer 1 is placed on an upper electrode, with its surface where the Al-Si electrode 7 is exposed down. The Al-Si electrode 7 whose side face 71 comes into contact with the wafer 1 is brought into contact with the upper electrode, whereby the impedance between the wafer 1 and a lower electrode is lessened and becomes constant. As a result, a passivation film 8 formed on the top becomes large in thickness, and the processed wafers are reduced in thickness variation to ±3%.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the semiconductor integrated circuit equipment characterized by to form the electrode layer which has the part which contacts a substrate at the periphery of the membrane-formation side of a semi-conductor substrate in the manufacture approach of semiconductor integrated circuit equipment equipped with the process which forms the wrap last passivation film in one electrode of a parallel pole for the whole-surface top of a substrate by the plasma-CVD method in support of a semi-conductor substrate by the periphery, to contact the front face of this electrode layer to one electrode of a parallel pole, and to perform a plasma-CVD method.
[Claim 2] The manufacture approach of the semiconductor integrated circuit equipment according to claim 1 formed in the part of the dummy chip which does not have a dimension as a design when a semi-conductor substrate is divided into two or more integrated circuit device chips for the electrode layer in contact with one electrode of a parallel pole.
[Claim 3] The manufacture approach of the semiconductor integrated circuit equipment according to claim 1 which forms the electrode layer in contact with one electrode of a parallel pole in a less than 2mm field from the periphery of a semi-conductor substrate.
[Claim 4] The manufacture approach of the semiconductor integrated circuit equipment according to claim 1 to 3 which carries out patterning of the electrode layer in contact with one electrode of a parallel pole to wiring and coincidence, and forms it in them from the metal layer formed on the whole semi-conductor substrate surface in order to use for wiring of the maximum upper layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is semiconductor integrated circuit equipment equipped with the process which forms the last passivation film which consists of Si3 N4, SiO2, a PSG, etc. using the plasma-CVD equipment of an parallel monotonous mold. (it omits Following IC) It is related with the manufacture approach.
[0002]
[Description of the Prior Art] As the environmental influence to IC is not received, in order to aim at stability of a property, the passivation technique which puts the insulator layer for protection on a circuit pattern is performed. It is necessary to perform membrane formation of such last passivation film at the low temperature 577 degrees C or less which is aluminum-Si eutectic temperature in order to avoid the effect to aluminum metal which is a wiring metal. Since membrane formation of SiN4 by the plasma-CVD method, SiO2, and PSG is performed at low temperature, it is a desirable approach.
[0003] Drawing 2 shows the polar zone of the parallel monotonous mold plasma-CVD equipment used for membrane formation of a up to [Si wafer] by the production process of IC. For example, the plate-like lower electrode 21 and the annular up electrode 22 with which the high-frequency voltage of 400V and 50kHz is impressed have countered up and down. The up electrode 22 is supported by the annular base material 23, and the silicon wafer 1 is laid on central opening. An electrical potential difference can be impressed between the bottom electrode 21 and 22 a top in this condition, and the passivation film can be formed on the front face of the wafer 1 maintained at predetermined temperature according to the heat source which is not illustrated by generating the plasma and making material gas react between a wafer 1 and the lower electrode 21.
[0004]
[Problem(s) to be Solved by the Invention] When the passivation film is formed by the plasma-CVD method shown in drawing 2 , thickness does not become homogeneity, for example, it is Si3 N4. There was a problem which many wafers with no less than 40% thinner than thickness expected in membranous thickness generate. This invention solves this problem and is to offer the manufacture approach of IC which can form the uniform last passivation film on a semi-conductor substrate.
[0005]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention shall form the electrode layer which has the part which contacts a substrate at the periphery of a semi-conductor substrate, contacts the front face of this electrode layer to one electrode of a parallel pole, and shall perform plasma CVD in the manufacture approach of IC equipped with the process which forms the wrap last passivation film in one electrode of a parallel pole for the whole-surface top of a substrate by the plasma-CVD method in support of a semi-conductor substrate by the periphery. When a semi-conductor substrate is divided into two or more integrated circuit device chips for the electrode layer in contact with one electrode of a parallel pole, it is desirable to form in the part of the dummy chip which does not have a dimension as a design, or to form in a less than 2mm field from the periphery of a semi-conductor substrate. And it is good to carry out patterning of the electrode layer to wiring and coincidence, and to form it in them from the metal layer formed on the whole semi-conductor substrate surface in order to use for wiring of the maximum upper layer.
[0006]
[Function] It turned out that expected thickness is not obtained by the passivation film which forms membranes by the plasma-CVD method for the RF impedance between a counterelectrode and a semi-conductor substrate becoming large, and discharge power declining for the resistance in the contact section of a semi-conductor substrate periphery and an electrode. If the electrode layer which has a part in contact with a substrate is formed in a substrate periphery, this electrode layer is contacted to an electrode by low contact resistance and plasma CVD is performed in support of a substrate, since the high frequency impedance between a counterelectrode and a semi-conductor substrate will fall and it will become fixed, the last passivation film of expected thickness is obtained by homogeneity, and dispersion becomes small. This electrode layer can be formed in wiring and coincidence of the maximum upper layer of IC, and if it forms in the part of the dummy chip produced around a substrate, the number of IC chips obtained from one substrate will not decrease. Moreover, if the complicated mask for the electrode stratification is not needed but it forms that electrode layer in a less than 2mm field from a periphery in forming this electrode layer in a substrate periphery by fixed width of face, an electrode can be made to contact certainly, and there will also be little loss of the area of the significant part of a substrate, and it will end.
[0007]
[Example] Drawing 1 (a) It is a top view explaining the formation pattern of the silicon wafer in one example of this invention, and is drawing 1 . (b) (a) It is an expansion fragmentary sectional view in an A-A line. Drawing 1 (a) Setting, the silicon wafer 1 has a circular profile except for the part of an orientation flat 2. In order to obtain the chip of the dimension which is 20mmx20mm after the wafer process process performed about the wafer 1 whole is completed for example, it is cut in the shape of [of a die] an eye with the dicing lines 31 and 32 which intersect perpendicularly. Thus, the pattern with perfect IC is formed in the chip 4 of the range with which the slash is not drawn among the obtained chips in drawing. However, the chip whose periphery of a wafer 1 passes through the interior which drew and showed the slash by a diagram lacks some patterns of IC, and it becomes the dummy chip 5 at it. drawing 1 (b) from -- in this dummy chip 5, the aluminum-Si electrode 7 touches a part of exposure wafer side of the field of the dicing lines 31 and 32 which removed the oxide film 6 on the front face of a wafer 1 to the line, and were formed so that it may understand. The width of face of the contact surface 71 is 1 micrometers or more. As the field which this aluminum-Si electrode 7 has exposed is turned downward and it is shown in drawing 2 , a plasma-CVD method is installed on the up electrode 22, and is performed. When the aluminum-Si electrode 7 which touches the wafer 1 in respect of 71 contacts the up electrode 22, the impedance between a wafer 1 and the lower

electrode 22 falls, and it becomes a fixed value. (Consequently, the passivation film 8 4 formed by the upper part as shown in drawing, for example, Si3 N, Membranous thickness becomes thick and fits in less than **3% of dispersion of expected thickness between processing wafers.) In addition, since the aluminum-Si electrode 7 is not formed in the dicing line field 31 between the dummy chips 5, or the center section of 32, dicing is easily made like between the IC chips 4.

[0008] In order to form the pattern of such the dummy chip section Without using the mask with which the pattern for IC chip is uniformly formed in the range larger than the dimension of a wafer as carried out conventionally at each photograph process process The pattern for IC is exposed only into the part of the IC chip 4, and the pattern of an oxide film 6 and the pattern of the aluminum-Si electrode 7 protruded into opening of the oxide film 6 1 micrometers or more are exposed using two kinds of another photo masks in the dummy chip section 5. Patterning of the aluminum-Si electrode 7 is performed to patterning and coincidence of aluminum wiring of the maximum upper layer of the IC chip 4. [of a part] It is made for a resist not to remain in the dummy chip section at the time unrelated to patterning of an oxide film 6 and the aluminum-Si electrode 7 of a photograph process process. The above exposure can be performed even if it uses any of the stepping projection aligner which carries out projection exposure repeatedly, shifting a mask pattern using the adhesion which a mask is made to stick or approach a wafer and exposes it at once or a contiguity aligner, the mirror projection aligner which carries out the sweep of the line top using optical system, or a stepper.

[0009] It is in the condition that distribute to a wafer periphery and the wafer exposure exists as another example, and a negative form is used for the photoresist in the photograph process process at the time of aluminum wiring formation of the maximum upper layer, and there is a method of exposing apart from the mask exposure for IC pattern by the width of face more fixed than a wafer periphery to a less than 2mm field, and leaving aluminum electrode to the part. In this case, it is not avoided that a dummy chip arises to the field inside this aluminum electrode.

[0010]

[Effect of the Invention] According to this invention, by preparing the electrode which supports a substrate using the dummy chip part of the periphery of a semi-conductor substrate etc. at the time of a plasma-CVD method, and the electrode layer which contacts, the high frequency impedance could be reduced, the last passivation film of expected thickness was obtained with little dispersion, and reliable IC was able to be manufactured.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing explaining the formation pattern of the silicon wafer in one example of this invention, (a) Wafer top view, (b) (a) Partial expanded sectional view in an A-A line
[Drawing 2] The sectional view of the polar zone of parallel monotonous mold plasma-CVD equipment
[Description of Notations]
1 Silicon Wafer
31 32 Dicing line
4 IC Chip
5 Dummy Chip
6 Oxide Film
7 Aluminum-Si Electrode
8 Passivation Film
21 Lower Electrode
22 Up Electrode

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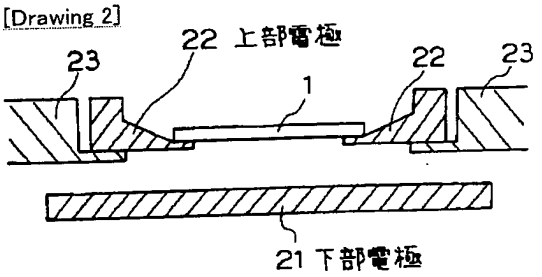
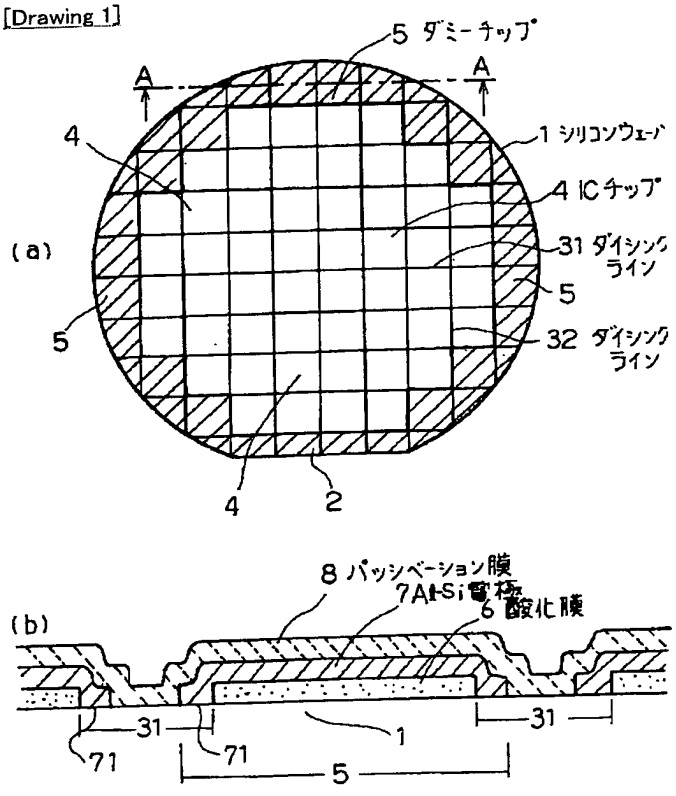
DRAWINGS

[Drawing 2]



[Drawing 1]



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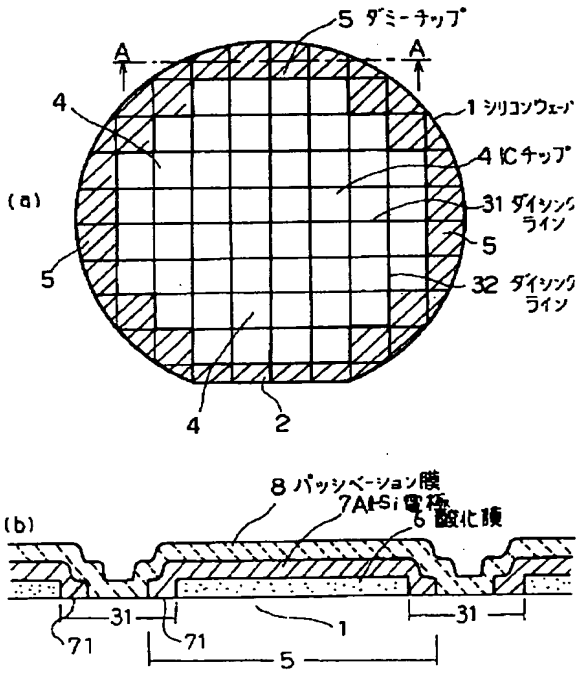
(54)【発明の名称】　半導体集積回路装置の製造方法

(57)【要約】
【目的】ＩＣチップの表面を覆うＳｉ，Ｎ，などの最終パッシベーション膜をプラズマＣＶＤ法で均一な所期の厚みに形成する。
【構成】平行平板電極の環状上部電極に支持する半導体基板の電極と接触する周辺部に、ＩＣのＡｌ配線形成と同時に電極層を形成する。これにより、基板と上部電極との間の接触抵抗が小さくなり、下部電極と基板との間の高周波インピーダンスが低下し、放電電力が増大するため、所期の厚さのパッシベーション膜が少ないばらつきで成膜される。



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【特許請求の範囲】

【請求項１】半導体基板を平行電極の一方の電極に周辺部で支持してプラズマＣＶＤ法により基板の一面上を覆う最終パッシベーション膜を形成する工程を備えた半導体集積回路装置の製造方法において、半導体基板の成膜面の周辺部に基板と接触する部分を有する電極層を形成し、この電極層の表面を平行電極の一方の電極に接触させてプラズマＣＶＤ法を行うことを特徴とする半導体集積回路装置の製造方法。

【請求項２】平行電極の一方の電極に接触する電極層を、半導体基板を複数の集積回路装置チップに分割した際に設計通りの寸法を有しないダミーチップの部分に形成する請求項１記載の半導体集積回路装置の製造方法。

【請求項３】平行電極の一方の電極に接触する電極層を半導体基板の外周より２ｍｍ以内の領域に形成する請求項１記載の半導体集積回路装置の製造方法。

【請求項４】平行電極の一方の電極に接触する電極層を、最上層の配線に用いるために半導体基板全面上に形成した金属層より配線と同時にパターニングして形成する請求項１ないし３のいずれかに記載の半導体集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、Si_3N_4、SiO_2、ＰＳＧなどよりなる最終パッシベーション膜を平行平板型のプラズマＣＶＤ装置を用いて成膜する工程を備える半導体集積回路装置（以下ＩＣと略す）の製造方法に関する。

【０００２】

【従来の技術】ＩＣに対する外界の影響を受けないようにして特性の安定を図るために配線パターン上に保護のための絶縁膜を被着するパッシベーション技術が行われる。そのような最終パッシベーション膜の成膜は、配線金属であるＡｌ金属に対する影響を避けるため、Ａｌ－Ｓｉ共晶温度である５７７℃以下の低温で行う必要がある。プラズマＣＶＤ法によるSiN_4、SiO_2、ＰＳＧの成膜は低温で行われるため、好ましい方法である。

【０００３】図２は、ＩＣの製造工程でＳｉウエーハ上への成膜に用いられる平行平板型プラズマＣＶＤ装置の電極部を示す。例えば４００Ｖ、５０ｋＨｚの高周波電圧が印加される平板状下部電極２１と環状上部電極２２が上下に対向している。上部電極２２は環状の支持体２３に支持され、中央の開口部上にシリコンウエーハ１が載置される。この状態で上、下電極２１、２２間に電圧を印加し、ウエーハ１と下部電極２１の間にプラズマを発生させて原料ガスを反応させることにより、図示しない熱源により所定の温度に保ったウエーハ１の表面上にパッシベーション膜を成膜することができる。

【０００４】

【発明が解決しようとする課題】図２に示したプラズマ

2

ＣＶＤ法によりパッシベーション膜を成膜した場合、膜厚が均一にならず、例えばSi_3N_4膜の厚さが所期の厚さより４０％も薄いウエーハが多数発生する問題があった。本発明は、この問題を解決し、半導体基板上に均一な最終パッシベーション膜を形成することのできるＩＣの製造方法を提供することにある。

【０００５】

【課題を解決するための手段】上記の目的を達成するために本発明は、半導体基板を平行電極の一方の電極に周辺部で支持してプラズマＣＶＤ法により基板の一面上を覆う最終パッシベーション膜を形成する工程を備えたＩＣの製造方法において、半導体基板の周辺部に基板と接触する部分を有する電極層を形成し、この電極層の表面を平行電極の一方の電極に接触させてプラズマＣＶＤを行うものとする。平行電極の一方の電極に接触する電極層を、半導体基板を複数の集積回路装置チップに分割した際に設計通りの寸法を有しないダミーチップの部分に形成するか、半導体基板の外周より２ｍｍ以内の領域に形成することが望ましい。そしてその電極層を、最上層の配線に用いるために半導体基板全面上に形成した金属層より配線と同時にパターニングして形成することが良い。

【０００６】

【作用】プラズマＣＶＤ法により成膜するパッシベーション膜に所期の厚さが得られないのは、半導体基板周辺部と電極との接触部における抵抗のために、対向電極と半導体基板との間の高周波インピーダンスが大きくなり、放電電力が低下するためであることがわかった。基板周辺部に基板と接触する部分を有する電極層を形成して、電極にこの電極層に低接触抵抗で接触させて基板を支持してプラズマＣＶＤを行えば、対向電極と半導体基板との間の高周波インピーダンスが低下し、一定になるため、所期の厚さの最終パッシベーション膜が均一に得られ、ばらつきが小さくなる。この電極層は、ＩＣの最上層の配線と同時に形成でき、基板周辺に生ずるダミーチップの部分に形成すれば、１枚の基板から得られるＩＣチップの数は減少しない。また、基板外周にこの電極層を一定の幅で形成する場合には、電極層形成のための複雑なマスクを必要とせず、その電極層を外周から２ｍｍ以内の領域に形成すれば、電極と確実に接触させることができ、基板の有効部分の面積の損失も少なくてすむ。

【０００７】

【実施例】図１（ａ）は本発明の一実施例におけるシリコンウエーハの形成パターンを説明する平面図であり、図１（ｂ）は（ａ）のＡ－Ａ線での拡大部分断面図である。図１（ａ）においてシリコンウエーハ１はオリエンテーションフラット２の部分を除いて円形の輪郭を持っている。ウエーハ１全体について行われるウエーハプロセス工程が完了したのち、例えば２０ｍｍ×２０ｍｍの

寸法のチップを得るため、直交するダイシングライン３１、３２で賽の目状に切断される。このようにして得られたチップのうち、図で斜線が引かれていない範囲のチップ４には、ＩＣの完全なパターンが形成されている。しかし、図で斜線を引いて示した内部をウエーハ１の外周が通過するチップには、ＩＣのパターンの一部が欠如しており、ダミーチップ５となる。図１（ｂ）からわかるように、このダミーチップ５においては、ウエーハ１の表面上の酸化膜６を線状に除去して形成されたダイシングライン３１、３２の領域の露出ウエーハ面の一部にＡｌ－Ｓｉ電極７が接触している。接触面７１の幅は１μｍ以上である。プラズマＣＶＤ法は、このＡｌ－Ｓｉ電極７が露出している面を下に向けて図２に示すように上部電極２２上に設置して行う。面７１でウエーハ１に接触しているＡｌ－Ｓｉ電極７が上部電極２２に接触することにより、ウエーハ１と下部電極２２との間のインピーダンスが低下し、一定の値になる。その結果、図に示すように上部に成膜されるパッシベーション膜８、例えばSi_3N_4膜の厚さは厚くなり、処理ウエーハ間で所期の厚さの±３％以内のばらつきにおさまる。なお、ダミーチップ５の間のダイシングライン領域３１あるいは３２の中央部にはＡｌ－Ｓｉ電極７が形成されていないので、ダイシングはＩＣチップ４の間と同様に容易にできる。

【０００８】このようなダミーチップ部のパターンを形成するには、従来行われているようにＩＣチップ用のパターンがウエーハの寸法より広い範囲で一様に形成されているマスクを用いないで、各フォトプロセス工程では、ＩＣチップ４の部分にのみＩＣ用のパターンを露光し、ダミーチップ部５には別の２種類のフォトマスクを用いて酸化膜６のパターン、その酸化膜６の開口部へ１μｍ以上はみ出すＡｌ－Ｓｉ電極７のパターンの露光をする。Ａｌ－Ｓｉ電極７のパターニングは、ＩＣチップ４の部分の最上層のＡｌ配線のパターニングと同時に行う。酸化膜６、Ａｌ－Ｓｉ電極７のパターニングに無関係のフォトプロセス工程の時には、ダミーチップ部にレジストが残留しないようにする。以上のような露光は、＊

＊マスクをウエーハに密着または近接させて一度に露光する密着あるいは近接露光装置、光学系を用いて一線上を掃引するミラー投影露光装置もしくはステッパを用いてマスクパターンをずらしながら繰り返して投影露光するステップ式投影露光装置のいずれを用いても行うことができる。

【０００９】別の実施例としては、ウエーハ周辺部に分散してウエーハ露出面が存在している状態で、最上層のＡｌ配線形成時のフォトプロセス工程におけるフォトレジストにネガ形を用い、ＩＣパターンのためのマスク露光と別にウエーハ外周より２ｍｍ以内の領域に一定の幅で露光してその部分にＡｌ電極を残す方法がある。この場合はこのＡｌ電極の内側の領域にダミーチップが生ずることは避けられない。

【００１０】

【発明の効果】本発明によれば、半導体基板の周辺部のダミーチップ部分などを利用してプラズマＣＶＤ法時に基板を支持する電極と接触する電極層を設けることにより高周波インピーダンスを低下させることができ、所期の膜厚の最終パッシベーション膜が少ないばらつきで得られ、信頼性の高いＩＣを製造することができた。

【図面の簡単な説明】

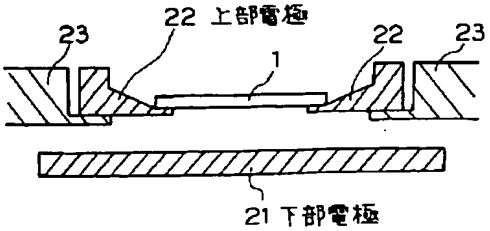
【図１】本発明の一実施例におけるシリコンウエーハの形成パターンを説明する図、（ａ）はウエーハ平面図、（ｂ）は（ａ）のＡ－Ａ線での部分拡大断面図

【図２】平行平板型プラズマＣＶＤ装置の電極部の断面図

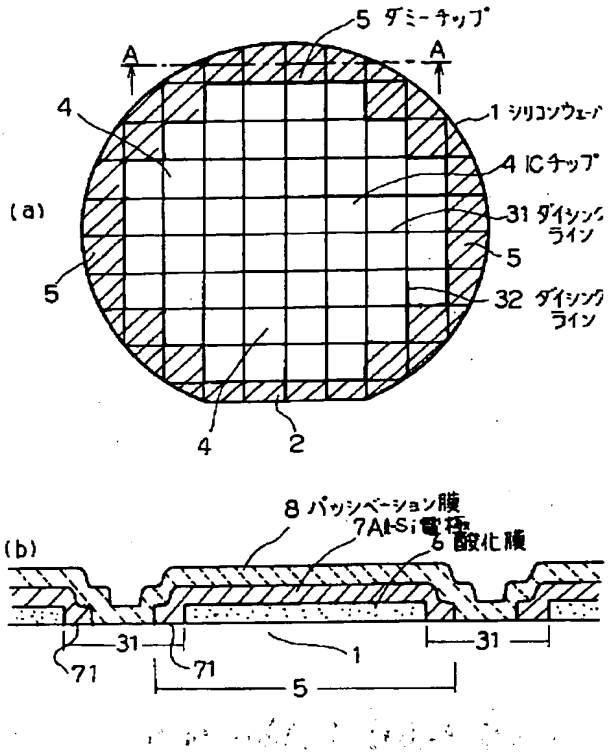
【符号の説明】

１　シリコンウエーハ
３１、３２　ダイシングライン
４　ＩＣチップ
５　ダミーチップ
６　酸化膜
７　Ａｌ－Ｓｉ電極
８　パッシベーション膜
２１　下部電極
２２　上部電極

【図２】



【図１】


5 ダミーチップ
A
A
4
1 シリコンウェーハ
4 ICチップ
(a)
31 ダイシング ライン
5
5
32 ダイシング ライン
4
2
8 パッシベーション膜
7 Al-Si電極
6 酸化膜
(b)
31
31
71
71
1
5